AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method comprising:
using a logic design component ~~data access primitive~~ to specify addressability for a memory-mapped device, addressability comprising an address matching function, a lane matching function and one or more bus connections,
specifying a first starting address for the memory-mapped device; and
replacing the logic design component ~~data access primitive~~ with logic components that implement a first set of addressing matching function, lane matching function and one or more bus connections for the memory-mapped device based upon the logic design component ~~data access primitive~~ and the first starting address.

2. (Currently Amended) The method of claim 1, further comprising replacing the logic design component ~~data access primitive~~ with logic components that implement a second set of addressing matching function, lane matching function and one or more bus connections for the memory-mapped device based upon the logic design component ~~data access primitive~~ and a second starting address.

3. (Currently Amended) The method of claim 1, further comprising:
coupling the logic design component ~~data access primitive~~ to the memory-mapped device; and
coupling an address bus to the logic design component ~~data access primitive~~.

4. (Original) The method of claim 3, wherein the addressing matching function compares an address from the address bus with the first starting address for the memory-mapped device.

5. (Original) The method of claim 4, wherein the first starting address is specified by a user.

6. (Original) The method of claim 4, wherein the first starting address is generated automatically.

7. (Original) The method of claim 6, wherein the first starting address is generated automatically using a set of address constraints.

8. (Currently Amended) The method of claim 1, wherein the logic design component ~~data access primitive~~ is selected to allow addressability for a minimum size transaction supported by the memory-mapped device.

9. (Original) The method of claim 8, wherein the memory-mapped device is a register.

10. (Currently Amended) A computer readable medium containing executable instructions which, when executed in a processing system, causes the processing system to perform a method comprising:

using a logic design component ~~data access primitive~~ to specify addressability for a memory-mapped device, addressability comprising an address matching function, a lane matching function and one or more bus connections,

specifying a first starting address for the memory-mapped device; and

replacing the logic design component ~~data access primitive~~ with logic components that implement a first set of addressing matching function, lane matching function and one or more bus connections for the memory-mapped device based upon the logic design component ~~data access primitive~~ and the first starting address.

11. (Currently Amended) The computer readable medium of claim 10, further comprising replacing the logic design component ~~data access primitive~~ logic components that implement a second set of addressing matching function, lane matching function and one or more bus connections for the memory-mapped device based upon the logic design component ~~data access primitive~~ and a second starting address.

12. (Currently Amended) The computer readable medium of claim 10, further comprising:
coupling the logic design component ~~data access primitive~~ to the memory-mapped device; and
coupling an address bus to the logic design component ~~data access primitive~~.

13. (Original) The computer readable medium of claim 12, wherein the addressing matching function compares an address from the address bus with the first starting address for the memory-mapped device.

14. (Original) The computer readable medium of claim 13, wherein the first starting address is specified by a user.

15. (Original) The computer readable medium of claim 13, wherein the first starting address is generated automatically.

16. (Original) The computer readable medium of claim 15, wherein the first starting address is generated automatically using a set of address constraints.

17. (Original) The computer readable medium of claim 10, wherein the memory-mapped device is selected to allow addressability for a minimum size transaction supported by the memory-mapped device.

18. (Currently Amended) A method, comprising:
selecting a logic design component ~~data access primitive~~ to provide data access of a desired transaction size, and to indicate an addressing matching function, a lane matching function and one or more bus connections for a memory-mapped device;
specifying an address constraint for the memory-mapped device;
instantiating a logic for the memory-mapped device, comprising:
generating a starting address for the memory mapped device using the address constraint;
using the selected logic design component ~~data access primitive~~ and the starting address to map the logic for the memory mapped device capable of being accessed at the desired transaction size, comprising:
generating first logic components that implement the address matching function, and
generating second logic components that implement the lane matching function and the one or more bus connections.

19. (Original) The method of claim 18, wherein the address constraint is specified by a user, and wherein the starting address for the memory mapped device is generated automatically.

20. (Original) The method of claim 18, wherein the transaction size is one in a group comprising a byte, a halfword and a word.

21. (Original) The method of claim 18, further comprising using a new starting address for the memory-mapped device without having to specify changes to the addressing function, the lane matching function and the one or more bus connections.

22. (Currently Amended) The method of claim 21, wherein different logic for the memory mapped device is instantiated automatically using the same logic design component ~~data access primitive~~ and the new starting address.

23. (Currently Amended) The method of claim 18, wherein the addressing matching function compares an address from an address bus coupled with the logic design component ~~data access primitive~~ with the starting address, and wherein when there is match, the lane matching function matching the transaction size of a transaction to a respective section of the memory-mapped device.

24. (Currently Amended) A computer readable medium containing executable instructions which, when executed in a processing system, causes the processing system to perform a method, comprising:

selecting a logic design component ~~data access primitive~~ to provide data access of a desired transaction size, and to indicate an addressing matching function, a lane matching function and one or more bus connections for a memory-mapped device;

specifying an address constraint for the memory-mapped device;

instantiating a logic for the memory-mapped device, comprising:

generating a starting address for the memory mapped device using the address constraint;

using the selected logic design component ~~data access primitive~~ and the starting address to map the logic for the memory mapped device capable of being accessed at the desired transaction size, comprising:

generating first logic components that implement the address matching function, and

generating second logic components that implement the lane matching function and the one or more bus connections.

25. (Original) The computer readable medium of claim 24, wherein the address constraint is specified by a user, and wherein the starting address for the memory mapped device is generated automatically.

26. (Original) The computer readable medium of claim 24, wherein the transaction size is one in a group comprising a byte, a halfword and a word.

27. (Original) The computer readable medium of claim 24, further comprising using a new starting address for the memory-mapped device without having to specify changes to the addressing function, the lane matching function and the one or more bus connections.

28. (Currently Amended) The computer readable medium of claim 27, wherein different logic for the memory mapped device is instantiated automatically using the same logic design component ~~data access primitive~~ and the new starting address.

29. (Currently Amended) The computer readable medium of claim 24, wherein the addressing matching function compares an address from an address bus coupled with the logic design component ~~data access primitive~~ with the starting address, and wherein when there is match, the lane matching function matching the transaction size of a transaction to a respective section of the memory-mapped device.